Abstracts

Integrated power transistor in 0.18-/spl mu/m CMOS technology for RF system-on-chip applications

Heng-Ming Hsu, Jiong-Guang Su, Chih-Wei Chen, D.D. Tang, Chun Hsiung Chen and J.Y.-C. Sun. "Integrated power transistor in 0.18-/spl mu/m CMOS technology for RF system-on-chip applications." 2002 Transactions on Microwave Theory and Techniques 50.12 (Dec. 2002 [T-MTT] (Special Issue on 2002 International Microwave Symposium)): 2873-2881.

A novel design and performance of a power MOS transistor for RF system-on-chip applications are reported. The power MOS transistor with high breakdown voltage is integrated into 0.18-/spl mu/m CMOS technology with only one additional mask. By an optimized design considering all aspects of DC and RF performances, a power MOS transistor with 16-GHz cutoff frequency and 24-GHz maximum oscillation frequency has been demonstrated. In addition, the power gain is 12 dB at 2.4 GHz with power-added efficiency of 50%. In this study, the device architectures that include drain engineering, substrate engineering, and gate scaling are investigated comprehensively.

❑ Return to main document.